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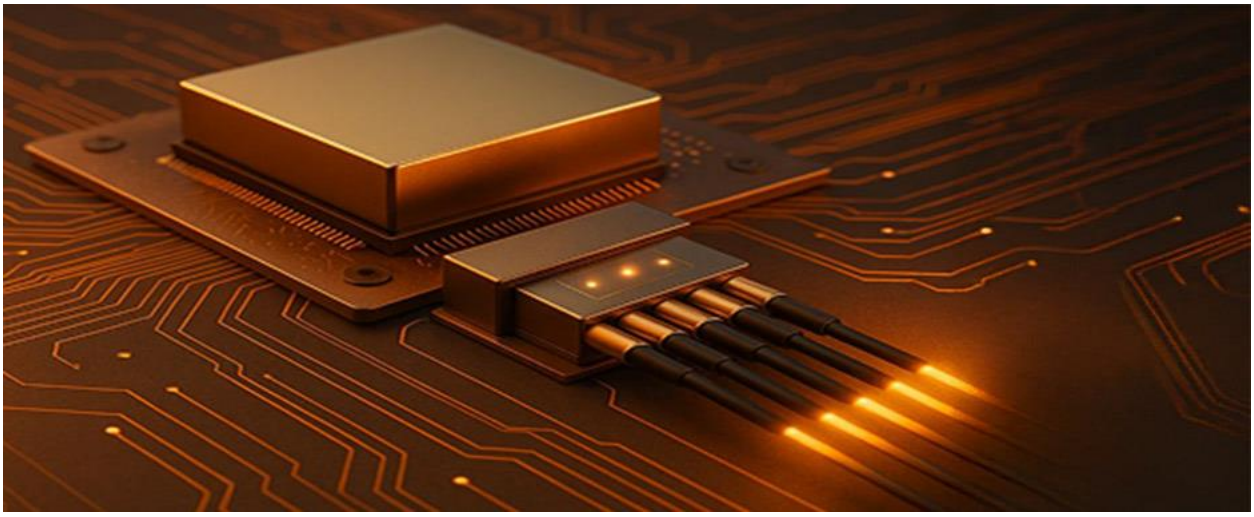
Co-Packaged Optics: From Breakthrough Concept to AI Infrastructure Reality



Co-packaged optics (CPO) is no longer an experimental idea reserved for research labs—it is rapidly transitioning into real-world deployment. With industry leaders like Marvell accelerating execution through strategic acquisitions, defined sampling timelines, and deep investments in custom silicon, advanced packaging, and photonics co-design, CPO is emerging as a foundational technology for next-generation AI networks.

Marvell's recent acquisition of Celestial AI and its roadmap to begin CPO sampling by 2027 send a clear signal to the market. Hyperscalers are no longer evaluating whether CPO will be necessary; they are actively planning how to build AI networks around it. As AI workloads continue to scale, traditional electrical interconnects are hitting hard limits in bandwidth density, latency, and power efficiency. Photonics—co-designed directly with compute and switching silicon—is becoming essential.

Why AI Data Centers Are Moving to Photonics

AI data centers are undergoing a fundamental architectural shift. Training and inference clusters now demand massive east-west traffic, ultra-low latency, and unprecedented

energy efficiency. Electronic interconnects struggle to meet these requirements beyond short reaches, especially as data rates climb and rack densities increase.

Photonic interconnects address these challenges by delivering higher bandwidth per millimeter, lower latency, and significantly improved power efficiency. Just as importantly, they enable carrier-class reliability from the rack level all the way to data center interconnect (DCI). This makes photonics indispensable not only for future scalability, but also for operational stability in production of AI environments.

The Packaging Bottleneck in Silicon Photonics

Despite its promise, CPO adoption is constrained by one critical factor: packaging. Silicon photonics introduces complexity at every level of integration. Challenges span laser and photodiode co-integration, photonic die packaging, optical alignment, and testability across modules and systems. Unlike conventional electronic packages, photonic packages must manage thermal, mechanical, optical, and electrical constraints simultaneously.

Testing remains a particularly thorny issue. Validating photonic components across wafers, packages, and systems requires new methodologies and tooling. Without a packaging-first approach, teams risk extended debug cycles, yield loss, and delayed time-to-market.

Designing for CPO from Day One

This is where deep expertise in custom packaging and system-level photonics co-design becomes essential. Custom chips demand custom packaging—and in the era of CPO, packaging cannot be an afterthought. Successful deployments start with architecture and partitioning decisions that explicitly account for photonics integration.

We support teams across the full CPO lifecycle, including architecture definition, CPO design-in, thermal and power modeling, signal integrity and power integrity analysis, and comprehensive packaging reviews. Beyond the hardware, we enable firmware and diagnostics bring-up, network operating system integration, and seamless transitions from pluggable optics to co-packaged implementations.

Our photonics portfolio and toolchains are purpose-built for AI-era requirements, optimizing bandwidth, efficiency, and reach while maintaining reliability. The result is fewer design iterations, reduced risk, and faster paths from concept to production.

Accelerating Custom Silicon and Fabric Integration

For organizations developing custom switch ASICs or accelerators—particularly advanced designs such as Byron-class chips that require photonics or fabric integration—we provide proven models, reference packages, and co-development workflows. These resources help minimize cost, reduce debug cycles, and preserve critical performance metrics like throughput and latency.

CPO adoption does not have to be a leap into the unknown. With the right collaboration and design strategy, teams can de-risk integration and accelerate their ramp to production-scale AI infrastructure—confident that their systems are built for the bandwidth and efficiency demands of the future.

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